UNITED STATES PATENT AND TRADEMARK OFFICE

SERIAL NO: 76/642036

MARK: C-RAM

CORRESPONDENT ADDRESS:
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GENERAL TRADEMARK INFORMATION:
http://www.uspto.gov/main/trademarks.htm

APPLICANT: BAE SYSTEMS Information and Electronic S ETC.

CORRESPONDENT'S REFERENCE/DOCKET NO:
N/A
CORRESPONDENT E-MAIL ADDRESS:

REQUEST FOR RECONSIDERATION DENIED

ISSUE/MAILING DATE:

Applicant is requesting reconsideration of a final refusal issued/mailed 5/14/07.

After careful consideration of the law and facts of the case, the examining attorney must deny the request for reconsideration and adhere to the final action as written since no new facts or reasons have been presented that are significant and compelling with regard to the point at issue.

The applicant states that "[t]here is absolutely no evidence of record that the relevant purchasing public understands the mark primarily as the common or class name for the goods." The examining attorney again points to the previously sent Internet evidence where various entities and publications discuss chalcogenide RAM and include its abbreviation C-RAM.

The applicant does go on to state that it uses the mark with the ™ symbol, however it is immaterial whether or not a generic term is used with a ™ symbol. Use of such a symbol on a generic term does not obviate the generic nature of the term. The purchasing public also comes in contact, likely moreso, with the previously sent evidence where the term is used in a generic manner by various entities. A two-part test is used to determine whether a designation is generic:

(1) What is the class or genus of goods or services at issue?

(2) Does the relevant public understand the designation primarily to refer to that class or genus of goods or services?

See H. Marvin Ginn Corp. v. International Ass'n of Fire Chiefs, Inc., 782 F.2d 987, 228 USPQ 528 (Fed. Cir. 1986); TMEP §1209.01(c)(i). Here, the goods are "radiation hardened computer and

semiconductor memory hardware and devices, namely, memory arrays featuring chalcogenide phase change material storage elements" or C-RAM as illustrated by the previously sent evidence.

Please also see new attached evidence showing use of the term in a generic manner in relation to the applicant's goods. Applicant may wish to respond with evidence showing that the term C-RAM is perceived by the purchasing public as a trademark of BAE Systems. Applicant has yet to supply any such evidence other than within its own publications.

Accordingly, applicant's request for reconsideration is *denied.* The time for appeal runs from the date the final action was issued/mailed. 37 C.F.R. Section 2.64(b); TMEP Section 715.03(c). If applicant has already filed a timely notice of appeal, the application will be forwarded to the Trademark Trial and Appeal Board (TTAB).

Note: The applicant did not supply use dates nor a complete allegation of use. The applicant did request registration on the Supplemental register, however, the examining attorney previously sent information stating that the mark is not eligible for registration on the supplemental register due to it being generic. Again, applicant may respond with evidence (other than its own publications) showing that the term is descriptive and not generic.

Applicant may wish to telephone the examining attorney at the number below for clarification.

/Kyle C. Peete/
Trademark Examining Attorney (Law Office 112)
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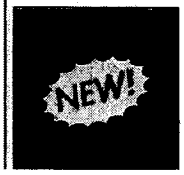
Vol 7 Number 3



COVER STORY: Data Storage: A Singapore Success Story

by Ng Ek Heng

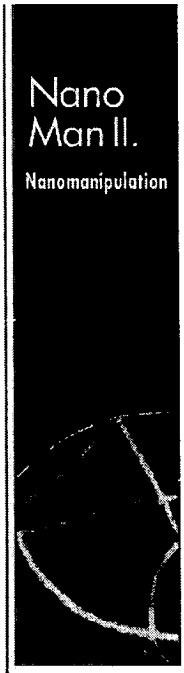
We live in an information age that sees data created with unprecedented speed. According to the School of Information Management and Systems at the University of California at Berkeley (www.sims.berkeley.edu/how-much-info), the world's total yearly production of print, film, optical, and magnetic content would require roughly 1.5 billion gigabytes of storage - the equivalent of 250 megabytes for each man, woman and child on earth. The need to store data thus created and accumulated has prompted the development of various storage media, such as the hard disk drive (HDD), the compact disc (CD) and the digital versatile disc (DVD).

Recognising the tremendous growth potential of data storage, Singapore has designated this sector as one that requires a key electronics-industry focus and introduced broad-ranging initiatives that have sharply enhanced its competitive position. These efforts have set the stage for the island nation to achieve outstanding success as a world-class innovation centre and manufacturing base for data storage products. Since the mid-1980s, the Republic has established a leading position worldwide in this niche market and is the largest producer of HDDs, generating more than 30% of the total global output. Today, the data storage industry represents the biggest sector within Singapore's electronics industry.

Data Storage Saved the Day

The importance of data storage has been heavily underscored by the devastating terrorist attack on the World Trade Center in New York City last September. In addition to the tragic human toll, the September 11 incident crippled businesses, with estimated losses totalling more than US$60 billion. Had this attack occurred before the information age, the US economy would have been brought to its knees by the unprecedented loss of information.

Incredibly, financial giant Morgan Stanley, the biggest tenant in the ill-fated towers, was up and functioning the very next day. This seemingly miraculous recovery can be



up and functioning the very next day. This seemingly miraculous recovery can be attributed to its practice of internal backup and copying of data instantaneously to a second location. The company capitalised on the convergence of computers and telecommunications to transmit massive amounts of information electronically for off-site storage.

Likewise, US financial markets took just one week to get back into business, a tremendous achievement considering the massive volume of data generated each trading day. Data storage not only allows organisations to backup information quickly and easily but also makes it possible to have remote access so that key personnel can operate at different locations.

From Computers to Consumer Electronics

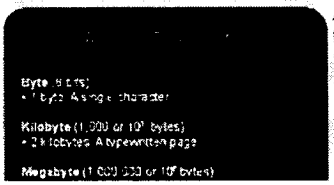
The successful recovery of information by US-based companies presents one critical dimension of data storage and its function in the business world. No less important is the storage of a database or personal information to an individual. In a rapidly networked world, we are all increasingly using personal data to carry out transactions and other daily activities by digital means.

Any kind of digital hardware - computer, consumer electronics, or household appliance - incorporates data storage in one form or another. Many digital products today must have basic information to function. The trend is moving towards increasingly "intelligent" digital devices that need greater information input, thus fuelling demand for yet more data storage products.

The data storage sector has been going through constant change to satisfy the demands of different niche markets. High-end enterprise users, for example, want high performance, competitive pricing, and ease of use in bundling together data storage products. The requirements differ for mainstream users who are price-conscious and satisfied with moderate performance and small-sized offerings. Mobile users prefer portable low-powered, moderate-performance storage devices, and aficionados of video applications want solutions that can operate quietly and smoothly deliver sustained video streams with lots of capacity.

Storage Technology

Whether in the form of hard disk, tape, optical disc or cards, data storage media stem from three main developments - magnetic, optical and volatile/non-volatile technologies. These all capitalise on the digital age wherein information - text, image, audio, video and multimedia - gets translated into a common binary language known as a "bit" (binary digit).



A bit is the smallest unit of data, and it can have two values, 1 or 0, of use only when combined with other bits to form a byte, comprising eight bits of data. For example, the character "a" is made up of one byte of data. A thousand bytes equal a kilobyte (KB), a million bytes a megabyte (MB), and 1,000MB one gigabyte (GB). In layman's terms, 1GB is equivalent to an entire

Source: University of California at Berkeley

volume of the Encyclopaedia Britannica or one typical television-quality movie (see table).

Staying on Top of Changes

Amidst fast-paced changes and storage-industry consolidation every two years, Singapore has held steadily to its strong position as a design and manufacturing base for storage products, particularly HDDs. In spite of the dwindling number of manufacturers - casualties resulted when companies became incapable of keeping up financially and technologically - the island nation continues to be the largest HDD producer, attracting the big names in the sector. It is noteworthy that the republic retains its pre-eminent position despite the intense competition from cost-competitive neighbouring countries.

The key to Singapore's success lies in its total approach strategy that involves initial economic and tax incentives, as well as all-rounded industry support and training, including value-added services such as a data storage research facilities. From fewer than 4 million units of HDDs produced in 1986, the annual output has been ramped up steadily to the current 50-million-unit level.

Realising that manufacturing strengths must be reinforced by other intrinsic capabilities, Singapore set up the Magnetics Technology Centre in 1992. In 1996 the centre was transformed into the Data Storage Institute (DSI) and its scope of research expanded to include optical storage technology (Figure 1). The move reflected Singapore's serious commitment to advancing the storage sector while attracting more storage-related companies to the country. DSI also actively spearheads strategic initiatives to effect technology transfer to the industry through collaboration and training.

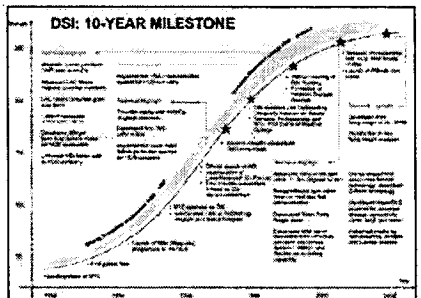


Figure 1: Milestones of the Data Storage Institute.

Guided by an international advisory panel with enthusiastic technologists from around the world, DSI quickly earned a reputation as a world-class institute. A report published by the Information Storage Industry Center, University of California at San Diego, ranked DSI as one of the top six research-and- development centres worldwide - and the only one outside the US and Japan. According to the institute's international advisory panel, four DSI research tracks already operate at world-class level; the advisory panelists believe that DSI has matching capabilities to plug the gaps in some of the leading US National Storage Industry Consortium programmes.

These endorsements of DSI's work have put Singapore on the international map as an innovation centre capable of taking data storage technologies to a higher level. DSI's research focus spans the various disciplines - magnetic disk drive, optical drive, non-volatile storage and network technologies.

Leading-Edge Research

Each year DSI undertakes some 30 collaborative research projects with both local and overseas storage companies. Besides projects that push technological limits to increase capacity and improve the performance of existing products, DSI pioneers research into new-generation technologies for data storage applications.

Hard Disk Drives

DSI's involvement in cutting-edge research will accelerate the exponential growth of storage density. Within an HDD, information is written, read or retrieved by magnetic heads flying over rotating disks containing data. The clearance between the head and the disk gets increasingly tight as the capacity increases and HDDs become smaller.

One yardstick by which to evaluate an HDD measures the data packed into it. Fifteen years ago it was 29 megabits (Mbits) per square inch; by the end of last year HDD manufacturers were reported to have packed 1,000 times more data into the same space. DSI is currently involved in research that will position a magnetic head less than 20 nanometres above the disk, a feat equivalent to flying a Boeing 747 smoothly less than 1cm above the ground with a fisherman standing on the aircraft, spearing 300 million fish per second.

DSI's staff also conducts research that will enhance the sensitivity of magnetic heads when reading data on the disk. Looking ahead, observers expect greater challenges, when data will be packed in at more than 100 gigabits (Gbits) per square inch. The era will come when a bit will be smaller than the critical dimension of the most advanced integrated circuit chip.

Improving on existing research underway in the area of spin-valve technology, DSI's researchers have obtained results that compare favourably with those of other organisations doing similar research. The institute is now working on the next generation of spin-valves based on its own design.

Non-Volatile Storage

Like human beings, some computer memories can retain information almost permanently whereas some lose information the moment power is switched off. The former is called non-volatile memory; the latter, volatile memory.

Many users know it takes time to boot up a PC. The machine needs time to load information from the hard disk every time it starts up because it uses random access memory (RAM), which is volatile. A solution in the offing lies in magnetic RAM (MRAM). Because of its many superior properties, such as non-volatility and short cycle time, MRAM is rapidly evolving into one of the most promising replacements for existing

MRAM is rapidly evolving into one of the most promising replacements for existing volatile memories. Moreover, it has potential as a cheaper alternative to other non-volatile memories, such as electrically erasable programmable read-only memory, or EEPROM.

DSI's current plans involve working on a multilayered MRAM that requires the use of only the active part of the cell without incorporating the whole transistor. The design helps to increase memory capacity and reduce manufacturing cost. In December 2000, IBM announced that it would jointly develop the MRAM technology with Infineon Technologies and hinted that a 256Mbit MRAM might be in production by 2004.

Another non-volatile memory device with promise is the **chalcogenide RAM** (C-RAM). Its successful development will be a personal computer user's dream. A computer utilising C-RAM could be turned off, then turned back on - immediately or 10 years later - and start right up where it left off.

Recent inexpensive developments have made it possible to use C-RAM as a practical high-performance memory device. DSI's researchers hope to understand better and capitalise on its properties for cost-effective manufacture of different digital products. C-RAM may one day pervade commercial memory products and revolutionise the entire computing industry, from smart appliances and desktop computers to consumer products not even invented yet.

Optical Drives

In the case of optical drives, the convergence of information, online entertainment and other emerging uses will require ultra-high data storage for homes and enterprises. Existing CD and DVD technologies have limited themselves to offering a maximum storage capacity of 650MB and 4.7GB, respectively. DSI's goal is to perform research that will take optical drives into the multigigabyte range with ever-higher levels of performance - research using different light sources, materials research, innovative coding schemes and systems design.

Next-Generation Data Storage

Technological breakthroughs constantly happen on the storage front, thus ensuring that existing products keep pace with the needs of users in terms of capacity and performance. These exciting new areas of research will lead to the development of next-generation data storage products.

Home-Networked Storage

Today, the phrase "era of home networking" constitutes more than just hype. The technologies exist for devices to connect, to communicate, and to exchange data in a home-networked environment. The world is quickly progressing towards a connected environment where many different devices will interconnect, with or without wires. However, a major component of this connected world still goes missing - information storage. Researchers can present a strong case for a single consolidated information storage device for the intelligently networked home, and one DSI project delves into the development of an appropriate storage solution for the home network.

Holographic Storage

Scientists currently focus attention on an exciting new and potentially revolutionary area - holographic memory. Holographic memory basically serves as an optical imaging technique that stores digital information three-dimensionally. Theoretically, the possibility exists of using holographic techniques, by means of a laser, to store a terabyte (TB) of data inside a crystal no larger than a sugar cube. 1TB (1,000GB) can be better understood by thinking of it as the equivalent of playing 62 days of continuous music or the storage of 1,000 copies of the complete Encydopaedia Britannica.

Although the basic concepts first underwent development in the 1960s, the lack of satisfactory recording media and key components throws up barriers to the development of practical holographic recording systems. DSI is looking at using new crystal material and laser research to find possible solutions to the problem.

Singapore continues to push the envelope to stay abreast of the developments in the data storage arena. With the combined efforts of the government, research institutes and industry, the Republic is poised to be a significant global player in this fast-changing and challenging field.

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Hardware Components

Semiconductor - Digital - ROM Memory IC Manufacturers

[DRAM] [SRAM] [RAM: other] [FLASH]
[EPROM] [EEPROM] [PROM / ROM: other]
[Memory Modules / Special]
[Home]

This is a listing of **Ovonics Unified IC Memory manufacturers**. Phase-change memory is a type of Non-Volatile memory.

Ovonics Unified Memory

No manufacturers yet, this is a new type of memory structure.

{Memory Chip Manufacturers Index}

IC Memory Acronyms listing.

Phase-Change Memory is also known as PCM, PRAM, PCRAM, Ovonic Unified Memory and Chalcogenide RAM, or C-RAM

{Memory Chip Manufacturers Index}

A listing of **Non-Volatile IC Memory manufacturers**. The types of products or devices they produce are listed under the company name, in alphabetic order. Additional electronic Equipment manufacturers may be found by selecting the OEM Equipment icon below, or component manufacturers may be found by selecting the Components icon below.

Home


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Software


Standards


Buses


Design


Reference

Last Modified 12/27/07

Systems and methods for measuring the useful life of solid-state storage devices

Brief Patent Description - **Full Patent Description** - Patent Application Claims Monitor Keywords

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to solid-state storage devices. More specifically, the present invention relates to systems and methods for measuring and monitoring the useful life of solid-state storage devices in operating environments.

[0003] 2. Description of the Related Art

[0004] Rotating hard disk drives (HDD) used, for example, in desktop, laptop, notebook, sub-notebook, tablet and

embedded computers support an industry-standard advanced technology attachment (ATA) command called Self Monitoring and Reporting Technology (SMART). The SMART function was designed to act as an "early warning system" for pending problems with mechanical media such as HDDs. The integrated controller on the HDD works in conjunction with various sensors to monitor a variety of different parameters within the HDD, such as mechanical wear of the HDD's spindle motor, to determine if any of the parameters are drifting from a norm that would indicate a possible problem with the HDD.

[0005] By contrast with HDDs, solid-state storage subsystems generally do not have moving parts. Thus, many of the parameters monitored by the SMART function used in HDDs are not applicable to solid-state storage subsystems. Solid-state storage subsystems generally include non-volatile storage components that can lose the ability to retain data stored thereon after approximately hundreds of thousands to approximately millions of write/erase cycles.

[0006] Generally, non-volatile storage components used in solid-state storage subsystems have a finite number of program/erase cycles (usually specified by component vendors as "endurance") that are recommended or guaranteed for proper data storage and retrieval. The number of such cycles varies by orders of magnitude based on the type of storage component used. Unfortunately, however, there is currently no method that can reliably determine or predict when the recommended or guaranteed endurance in a particular non-volatile storage component will be exceeded. Thus, solid-state storage subsystems are often allowed to operate beyond the specified endurance until a failure occurs, causing unscheduled system down time and potentially significant data loss.

SUMMARY OF THE INVENTION

[0007] Thus, it would be advantageous to develop a technique and system for reporting information from a solid-state storage subsystem to a host system that uses the information to measure or determine the useful life remaining in the non-volatile storage components of the solid-state storage subsystem.

[0008] The present invention comprises a non-volatile solid-state storage subsystem designed to internally maintain usage statistics information reflective of the wear state, and thus the remaining useful life, of the subsystem's memory array. The storage subsystem may, for example, be in the form of a detachable or removable device that plugs into, and receives power and commands via, a standard slot or port of a host computer system. In one embodiment, the storage subsystem supports one or more commands for enabling the host system to read the usage statistics information, or data derived therefrom, to evaluate the subsystem's remaining life expectancy. The host system may use this information for various purposes, such as to display or report information to a user regarding the remaining life of the subsystem, and/or to vary a subsystem usage policy (e.g., to avoid storing mission critical data on a device that is near the end of its useful life).

[0009] Neither this summary nor the following detailed description purports to define the invention. The invention is defined by the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] A preferred embodiment of the invention will now be described with reference to the drawings summarized below, which are intended to illustrate, and not limit the present invention.

[0011] FIG. 1 is a is a block diagram illustrating a host system linked to a solid-state storage subsystem according to one embodiment of the invention.

[0012] FIGS. 2A and 2B illustrate examples of meter displays that may be generated by the host system to indicate the amount of useful life remaining in the solid-state storage subsystem.

[0013] FIG. 3 illustrates a process that may be used to calculate the amount of useful life remaining in the solid-state storage subsystem.

[0014] FIG. 4 illustrates one example of how the non-volatile memory of the storage subsystem may be arranged.

[0015] FIG. 5 is a graph illustrating the relationship between the life used of a solid-state storage device and the spare data blocks remaining in the solid-state storage device.

[0016] FIG. 6 shows a host system in communication with a plurality of solid-state storage subsystems.

[0016] FIG. 6 shows a host system in communication with a plurality of solid-state storage subsystems.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

[0017] A solid-state storage subsystem, and associated processes that may be implemented by a host computer, will now be described with reference to the drawings. This description is intended to illustrate a preferred embodiment of the invention, and not limit the invention. The invention is defined by the claims.

I. Overview

[0018] FIG. 1 is a block diagram illustrating a host system 110 connected to a solid-state storage subsystem 112 according to one embodiment of the invention. The host system 110 comprises a computer such as a personal computer, workstation, router, blade server or other type of computing device. For example, the host system 110 may be a military system, a flight computer or other flight avionics system, a wearable computer used for military applications, a high-speed data recorder, a medical device, an industrial control system, an interactive kiosk, a personal digital assistant, a laptop computer, an interactive wireless communication device, a point-of-sale device, or the like. The host system 110 stores data on the solid-state storage subsystem 112, and may provide operating system functionality and a boot process for the subsystem 112. The host system 110 executes a driver program 113 that provides functionality for communicating with the subsystem 112, such as by issuing commands in accordance with an ATA or other standard.

[0019] The solid-state storage subsystem 112 comprises a controller 114 and a non-volatile memory (NVM) array 116. The NVM array may, but need not, be implemented using NAND memory components. As is conventional, the controller 114 is configured (typically via firmware) to write data to, and read data from, the NVM array in response to commands from the host 110. The controller also preferably implements a wear-leveling algorithm, as is known in the art, to distribute write operates across memory blocks of the NVM array. The storage subsystem 112 may be in the form of a detachable device and may communicate with any standard or unique communications interface, including but not limited to parallel, serial ATA, IEEE, RS232/423, PCMCIA, USB, Firewire (IEEE-1394), FibreChannel, or PCI Express bus. The storage subsystem 112 may also receive its power from the host over this bus.

[0020] As discussed in detail below, as the controller 114 performs write operations to the memory array 114, it updates a non-user-data area of the array (i.e., an area not exposed to the host's operating system) with usage statistics information reflective of the number of program/erase cycles that have been executed. This information preferably includes a set of counters, with different counters corresponding to different blocks or areas of the memory array; however, the usage statistics may be maintained in any of a variety of formats. These counters are initially set to zero (or some other selected starting value) when the device is manufactured or first initialized, and are incremented over time as program/erase cycles are performed. In some embodiments, the usage statistics data stored in the memory subsystem 112 also includes timestamps, or other temporal data, received from the host; this temporal data may be used to calculate the useful life of the subsystem 112 in terms of time (e.g., days and hours), as may be desirable for some applications.

[0021] In addition to industry standard commands, the controller 114 supports, and the driver 113 issues, one or more vendor-specific commands that provide host access to some or all of the usage statistics information. The controller 114 may provide the usage statistics data to the host in its raw format, and/or in a summarized or aggregated form. The host system 114 may use the retrieved usage statistics in a variety of ways so as to reduce the likelihood of data loss. For example, the host system, via the driver 113 or another software component, may display information, such as a gauge (see FIGS. 2A and 2B, discussed below), reflective of the remaining life of the subsystem 112. The host system may also trigger an alert message to indicate that preventive maintenance will be required at a certain time in the future.

[0022] Users may use the reported information in a variety of ways. For example, based on historical usage and the predicted amount of useful life remaining, a user may decide to replace the storage subsystem 112 during a regularly scheduled maintenance of the host system. As another example, the resale value of the host system 110 and/or the solid-state storage 112 system may be based at least in part on the useful life remaining in the solid-state storage subsystem.

[0023] As another example of how the retrieved usage data may be used, the host system 110 may be programmed to use the usage data to adjust its use of the subsystem 112. For instance, as discussed in further detail below, in a host system that periodically logs data to the solid-state storage subsystem 112, the host 110 may reduce the frequency with which it logs such data as the subsystem approaches the end of its useful life. The host system may also vary its usage policy so that mission critical data is only stored on a subsystem that has not yet reached a particular wear threshold, such as 75%.

[0024] Thus, the user and/or the host system 110 can reduce or eliminate the cause of solid-state storage subsystem endurance-related failures. In one embodiment, for example, the host system or user can set a wear threshold that, when met, indicates that the solid-state storage subsystem is in need of preventative maintenance and/or replacement. In addition, or in other embodiments, the host 110 can use data from two time periods and their respective timestamps to calculate the remaining lifespan of the storage subsystem 112. For example, as discussed below, the driver 113 may be configured to periodically write a timestamp to the subsystem 112 (or another storage device) together with information about the subsystem's current wear level, data usage information or endurance data collection, and to retrieve and analyze this information to predict the amount of time before the subsystem fails.

[0025] The storage subsystem 112 may, for example, be a solid-state memory card that plugs into a slot of the host system 110 and complies with at least one of the following card specifications: CompactFlash, PCMCIA, SmartMedia, MultiMediaCard, SecureDigital, Memory Stick, ATA/ATAPI. The storage subsystem 112 may, for example, have a housing and signal interface that complies with one of the following specifications: sub 1 inch hard disk drive, 1.8 inch hard disk drive, 2.5 inch hard disk drive and 3.5 inch hard disk drive. A custom form factor and/or signal interface may alternatively be used.

[0026] In one embodiment, the controller 114 executes a firmware program to perform processes as described herein and comprises an ATA flash disk controller available from Silicon Storage Technology, Inc. of Sunnyvale Calif. as part number SST55LD019A. The controller 114 may alternatively be implemented using another type of device, such as an application-specific integrated circuit (ASIC), or may comprise multiple distinct devices. Further, although the controller 114 preferably executes firmware, a controller that does not execute a firmware program may be used.

[0027] The NVM array 116 comprises a plurality of solid-state storage devices 118 coupled to the controller 114. The solid-state storage devices 118 may comprise, for example, flash integrated circuits, Chalcogenide RAM (C-RAM), Phase Change Memory (PC-RAM or PRAM), Programmable Metallization Cell RAM (PMC-RAM or PMCm), Ovonic Unified Memory (OUM), Resistance RAM (RRAM), NAND memory, NOR memory, EEPROM, Ferroelectric Memory (FeRAM), or other discrete NVM chips. The solid-state storage devices 118 may be physically divided into blocks, pages and sectors, as is known in the art.

[0028] The host system 110 exchanges control signals 122 with the controller 114 to coordinate the reading and writing of data to and from the solid-state storage devices 118. The controller 114 handles the read and write operations by sending memory control signals 120 to the NVM array 116. The control signals 122 may include, for example, read commands and write commands. The control signals 122 may be used to send commands selected from, for example, industry standard command sets such as those provided by ATA, CF card or PC card standards to read from or write data to standard storage devices. The host system 110 also exchanges data signals 124 with the controller 114. The data signals may include, for example, data to be written to the NVM array 116, data read from the NVM array, and monitored data, as discussed below.

[0029] To retrieve some or all of the stored usage statistics data, the host system 110, via the driver 113, sends a defined sequence of vendor-specific commands to the controller 114. In some cases, the host system 110 may transmit this data, or information derived therefrom, over a computer network to another node.

II. Example User Interface

[0030] FIG. 2A illustrates one example of a meter or gauge 200 that may be generated by the driver 113, or another software component, to indicate the amount of useful life remaining in the solid-state storage subsystem 112. In this example, a pointer 202 in the meter display 200 indicates the wear state or "utilization" of the NVM array 116 relative to a percentage scale 204. If the pointer 202 points to 0%, for example, substantially all of the specified endurance or number of program/erase cycles recommended or guaranteed for the NVM array 116 remain. If, however, the pointer 202 points to 100%, the specified endurance of the NVM array 116 has been reached and the probability of a failure is very high.

[0031] As shown in FIG. 2A, the meter display 200 in this example also includes a threshold indicator 206 displayed relative to the percentage scale 204 so as to indicate an upper limit or threshold set by the host system 110 or a user. The threshold is advantageously set below a specified data endurance or wear level so as to reduce the probability of a failure. In one embodiment, a warning signal is provided once the pointer 202 reaches the threshold indicator 206. The driver 113 may prevent the host system 110 from performing additional write operations to the subsystem 112 once this or some other threshold has been reached.

[0032] In the example shown in FIG. 2A, the time indicator 208 is a sliding time window of six months starting from a current

time corresponding to a current location of the pointer 202 and extending back in time for six months. Thus, by observing the percentage of available program/erase cycles used during the past six months, for example, the host system 110 or user can predict when the pointer 202 will reach the threshold indicator 206 and/or the specified endurance limit (e.g., 100%) and display or otherwise output this prediction to a user. Various other types of time indicators can be used. For example, in another embodiment, the time indicator 208 starts at 0% and ends at the pointer 202 while incrementing the displayed time (e.g., 1 day, 2 weeks, 4 months, etc.).

[0033] Other types of displays may also be used, such as the status bar shown in FIG. 2B. The status bar 220 grows as the percentage of specified endurance for the NVM array 116 is used. As shown in FIG. 2B, in certain such embodiments, the status bar 220 includes a displayed percentage 222 of specified endurance used. In other embodiments, the percentage is displayed as a scale along the length of the status bar 220.

[0034] In some embodiments, the storage subsystem 112 may itself be configured to display information about its current wear state. For example, the storage subsystem may include a small LCD or other display that generates a gauge image similar to that shown in FIG. 2B, or which displays a value or symbol reflective of the wear level, data endurance or life expectancy of the device. In such embodiments, the ability for the host 110 to read the stored usage data may optionally be omitted.

III. Calculation of Remaining Useful Life

[0035] FIG. 3 illustrates a sample process for determining the wear level of a solid-state storage subsystem 112 according to one embodiment. The illustrated steps may be performed solely by the controller 114 in response a command or command sequence from the host, or may be performed partially by the controller 114 and partially by the driver/host. In step 301, the controller 114 reads the block counters for each of the 128 k memory blocks in the memory array 116. Each such counter value indicates the number of program/erase cycles experienced by the respective block. As discussed below in connection with FIG. 4, the block counters 408 may be maintained in non-user-data areas of their respective blocks 402. Next, in step 302 the valid blocks are identified. In certain embodiments, a valid block is identified by the controller 114 by determining which blocks are invalid. During a write or erase procedure the controller 114 may attempt to write or erase a page or a block; if an error is returned to the controller 114, the controller 114 will try a second attempt. If the second attempt also fails to return the proper data or error correction code (ECC) 420, then the block will be marked as an invalid block.

[0036] In step 303, the counter values of the valid blocks are summed. The number of valid blocks is also multiplied by 2,000,000 in step 304 to determine the total number of possible writes for the solid-state storage subsystem 112. The 2,000,000 value reflects the number of erase cycles specified as the endurance of most solid-state storage device 118, any may be varied significantly to accommodate different types of memory devices. In other embodiments, the value may be set below this common value so as to reduce the risk of losing data due to a failure. For example, in some embodiments, the threshold is set in a range between approximately 70% and approximately 90% of the specified endurance of the solid-state storage. Finally, in step 305, the sum of the block counters from step 303 is divided by the total number of possible writes from step 304 to estimate the amount of useful life remaining in the storage subsystem 112 as a percentage.

[0037] The ATA interface allows vendors to create vendor-specific commands in order to properly engage with the hardware the vendor manufactures for an ATA interface. In certain embodiments discussed herein, in addition to industry standard commands, the controller 114 supports, and the driver 113 issues, one or more vendor-specific commands that provide host access to some or all of the usage statistics information, such as reading counter information for data blocks. Furthermore, one or more vendor-specific commands may provide the host access to information regarding the number of invalid blocks.

IV. Organization of Memory Array

[0038] FIG. 4 illustrates the physical data structure 300 of a solid-state storage device 118 according to one embodiment. As will be recognized, the arrangement of data elements in FIG. 4 represents only one of many possible arrangements that can be used to practice the invention. The data structure 300 is divided into a plurality of data blocks 402 (Block 0 and Block 1 are shown) and spare data blocks 404. The data blocks 402 are further divided into a plurality of pages 406. Pages are further divided into a plurality of sectors 414.

[0039] In the example shown in FIG. 4, the data blocks 402 are 128-kBytes, the pages 406 are 2-kBytes and the sectors are 512-Bytes. The data blocks 402, pages 406 and sectors 414 can, of course, have other sizes. An artisan will also recognize

512-bytes. The data blocks 402, pages 406 and sectors 414 can, of course, have other sizes. An artisan will also recognize that individual bytes typically are not be written or programmed into a sector 414 of a solid-state storage device 118. Rather, entire sectors 414 or pages 406 are generally programmed at the same time. Further, the sectors 414 or pages 406 are cleared of any previous data before being programmed with any new data. Generally, an entire data block 402 is erased at the same time.

[0040] One data storage method is to map logical addresses to fixed physical locations on the solid-state storage devices 118. However, when a host application updates the same data repeatedly, direct mapping can quickly cause one or more data blocks 402 to wear out due to the large number of program/erase cycles. Repeatedly updating the same group of sectors is common. For example, file systems generally maintain data that describes the allocation of sectors 414 to files. Such data is generally located in a predetermined area on a solid-state storage device 118.

[0041] To prevent failures due to repeated program/erase cycles in high-volume locations, the controller 114 remaps logical data to spare data blocks 404 when a particular data block 402 reaches its limit of specified endurance. When using spare data blocks 404 for this purpose, the remaining useful life of the NVM array 116 is directly related to the number of spare data blocks 404 remaining. For example, FIG. 5 is a graph illustrating the relationship between the life used of a solid-state storage device 118 and the spare data blocks 404 remaining in the solid-state storage device 118. The line 502 illustrates that the useful life of the solid-state storage device 118 can be measured by the number of remaining spare data blocks 404. For example, when 50% of the spare data blocks 404 have been used, 50% of the solid-state storage device's 118 life has been used.

[0042] However, the common use of wear leveling makes it more difficult to predict the amount of life remaining in a solid-state storage device 118. Wear leveling is generally used to map the same logical data to different physical locations. Thus, program/erase cycles can be evenly spaced across the NVM array 116. Wear leveling may include, for example, monitoring the number of program/erase cycles for the data blocks 402 and changing the logical-to-physical address mapping of one or more data blocks 402 so as to direct future high-volume re-writes to data blocks 402 that have historically been used less often. Thus, the spare data blocks 404 are not generally used until the program/erase cycles have been spread across the data blocks 402 such that a large number of the data blocks 402 have reached their specified endurance limit. When the number of spare data blocks 404 falls below a selected threshold, the controller 114 may, in some embodiments, be configured to interrupt and send a notification message to the host system 110.

[0043] Referring again to FIG. 5, when using wear leveling, the line 504 illustrates that monitoring the number of spare data blocks 404 remaining is not a good predictor of the percentage of life used because spare data blocks 404 do not begin to be used until a large number of data blocks have reached their specified endurance limit. Thus, the number of spare data blocks 404 declines rapidly toward the end of the useful life of the solid-state storage device 118. Therefore, adequate warning of the end of the useful life typically cannot generally be provided by monitoring the number of spare data blocks 404 remaining.

[0044] In the illustrated embodiment, a predetermined page in a data block 402 is designated as a block counter 408 used by the controller 114 to store monitored data. In certain embodiments discussed herein, the block counter 408 may store the number of times substantially the data block was erase. The block counter 408 may also store the number of times substantially all the data blocks 402 in the NVM array 116 are erased, the number of times substantially all the data blocks 402 in a corresponding solid-state storage device 118 are erased, the number of data blocks 402 that are at or near a threshold value, the number of spare data blocks 404 used, combinations of the foregoing, or the like. In certain embodiments, the block counter 408 may be kept in any storage area generally not accessible by an end user using logical block addressing access.

[0045] In order to implement wear-leveling, data is written to pages 406 in a first block 300 until all available pages in the first block 300 store data. As each page 406 is written, its write counter 416 is incremented. When the first block 300 is full, the data is moved to a second block, the first block 300 is erased, and the first block's threshold counter 412 is incremented. After a threshold value is met, the erase counter 410 is incremented and the threshold counter 412 is reset. The combination of the erase counter 410 and the threshold counter 412 make up the total number value for the block counter 408.

[0046] Although the usage data is maintained in the NVM array 116 in the preferred embodiment, the controller 114 could alternatively store this data is a separate non-volatile memory. For example, the controller 114 could include its own internal non-volatile memory that is used for this purpose, or could access a separate NVM array that is used to store such status information.

information.

[0047] In one embodiment, the controller 114 outputs the raw conductor data to the host system 110, and the driver 113 analyzes this data to determine, for example, the amount of life left in the NVM array 116 and/or individual solid-state storage devices 118. The driver 113 may also predict, for example, when the NVM array 116 will likely reach its overall specified endurance. As mentioned above, the controller 114 may alternatively perform some or all of the analysis of the counter data, and output the result to the host 110.

[0048] In certain embodiments, usage is also tracked at the page 406 and/or sector 414 levels. Returning to FIG. 4, the magnified data sector 422 illustrates a data structure including one or more counters 416 for maintaining data used to measure the remaining life of the NVM array 116 and/or the corresponding solid-state storage device 118. The sector 422 also includes an identification (ID) 418 representing a physical address of the sector 422 and ECC 420 including data for detecting and correcting errors in user data sectors 414. In certain embodiments, as shown, the data structure 422 housing the counter 416, ID 418, and ECC 420 is composed of four 16-Bytes which are usually not accessible in the readable-writeable area of the NVM.

[0049] The one or more counters 416 include, for example, a revision counter representing the number of times the controller 114 has written to the particular sector 414 and an erase counter representing the number of times the controller 114 has erased the corresponding data block 402. In addition, or in other embodiments, the counters 416 include a pointer to the location of the counter 408 in the data block 402. The controller 114 accesses monitored data from one or more of the counters 408, 416 in response to a command from the host system 110. The host system 110 may request the monitored data at any time, as part of a background process, and/or on a polling schedule (e.g., hourly, daily, and/or monthly). In certain embodiments, the controller 114 accesses monitored data directly from the counters 416 in the sectors 414. In other embodiments, the controller 114 accesses monitored data from both the counters 416 in the sectors 414 and the counters 408 in the data blocks 402.

[0050] The magnification of the block counter 408 illustrates a data structure configured to track erase cycles for a data block 402 according to an embodiment. This data structure may be generated and maintained by the controller 114 via execution of a firmware program. The block counter 408 includes an erase counter 410 and a threshold counter 412. The erase counter 410 is incremented each time the data block 402 is erased. The threshold counter 412 is incremented when the erase counter 410 reaches a predetermined threshold. When the threshold counter is incremented, the controller 114 performs wear leveling on the corresponding data block 402 by remapping corresponding logical addresses to different physical locations in other data blocks 402.

V. Example Applications Involving Multiple Subsystems

[0051] FIG. 6 shows a host system 110 in communication with a plurality of solid-state storage subsystems 112 of the type described above, and will be used to describe some additional applications for the usage statistics information. The host system 110 runs a storage manager program 615, which may include or communicate with a device driver 113 (FIG. 1) as described above. The storage manager reads the raw or processed usage data from each of these subsystems 112, and may use this data in various ways.

[0052] For example, the storage manager 615 may use the usage data to perform wear leveling at the device or subsystem level. For instance, where two solid-state storage subsystems 112 are connected to the host system 110, and the first storage subsystem 112 has more wear than the second, the storage manager 615 may choose to direct data storage to the second subsystem so as to reduce wear on the first storage subsystem 112. The storage manager may also attempt, where possible, to store infrequently-changing data to the first storage subsystem, while directing data that changes relatively frequently to the second storage subsystem.

[0053] The storage manager 615 may additionally or alternatively differentiate between critical and non-critical data. For example, the storage manager 615 may choose to store less critical data on a device 112 with more wear and to store more critical data on a device 112 with less wear. Application programs that generate or supply such data may notify the storage manager of the data's type (e.g., critical versus non-critical) at the time a write operation is requested. The storage manager 615 may differentiate between critical and non-critical data during every write to the storage subsystems 112, or at other configurable times.

[0054] While certain embodiments of the inventions have been described, these embodiments have been presented by way

[0054] While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the invention. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms. Furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

Brief Patent Description - **Full Patent Description** - Patent Application Claims
Click on the above for other options relating to this Systems and methods for measuring the useful life of solid-state storage devices patent application.

Related Patent Applications:

20070288589 - Usb apparatus and control method therein - The present invention relates to an application of the Universal Serial Bus (USB) technology, and more particularly, to a USB apparatus with data storage and security token and control method therein. In an embodiment of the present invention, both mass storage and security token are implemented in a USB apparatus ...

Previous Patent Application:
System and method for caching sequential programs
Next Patent Application:
Multi-level content addressable memory
Industry Class:
Electrical computers and digital processing systems: memory

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THURSDAY, SEPTEMBER 6, 2007

Enough RAM??

Definition of RAM

Memory is one part of the computer that acts as storage for computer's instructions as well as data. Data or instructions can be inputted or write into and accessed or read from the memory. There are two types of memory involved, which are known as read only memory or ROM and random access memory or RAM. ROM enables data or instructions only to be read whereas RAM is both writable and readable. However, we will focus only on matters related to RAM.

RAM is a memory module made in the form of integrated circuits plugged in on the motherboard of a computer via a socket. Data stored in it, can be randomly and easily moved or accessed without involving any physical movement of storage medium or reading head

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from the physical location. Data signals are channeled back and forth through RAM bus from and into RAM. RAM bus acts as a highway that connects RAM to the other parts of the computer, which enables the signals transmission.

CHARACTERISTICS OF RAM

RAM is characterized as a volatile memory. Volatile means that data is lost once the electricity is off. This is one of the reasons why a computer needs a secondary storage which is non-volatile such as hard disk, writable CD-ROM, flash memories and so on.

The fact that RAM comes in handy because of it smaller size compares to the other storage medium; it is easy to upgrade RAM by just slot in onto the socket of the motherboard and surely it does not consume too much of the space area. The retrieval times of the data are also short compared to the other memory because it does not require any physical movement.

Bits and bytes measure capacity of RAM. Such small chip is used as a working area to retrieve, load, display, and manipulate data and instructions or application from and to its memory locations.

In order to ensure data integrity, certain RAM can also detect or corrects memory errors on the data by using RAM parity or error correction codes (ECC). Parity is a method used to detect errors while ECC can both detect and correct errors. However, ECC is commonly used in servers and high-end computers.

There is a part of RAM that integrated with the central processing unit (CPU) of a computer. It is called cache memory. It jobs is to supply the CPU with the most frequent used instructions as fast as it can to fasten and smoothen the CPU processes.

TYPES OF RAM and COMPARISON WITH OTHER SYSTEMS

1. DRAM

Dynamic random access memory (DRAM) was introduced in early

1980s, as a type of RAM that hold data for a short period of time. The chips are made of tiny capacitors, which are chargeable and dischargeable, and it has to be refreshed frequently to avoid data from lost.

It can be easily found in 8MB, 16MB, 32MB, 64MB and so on depends on its storage size. The access time is rated in nanoseconds such as 60ns, 70ns and many more. It requires 60 billionths of a second in order to save or return to the requested information. The lower the nanospeed, the faster the memory can get it job done.

The two smaller versions of DRAM modules namely Small Outline DIMM (SO_DIMM) and Small Outline RIMM (SO-RIMM) are used in laptops. For higher capacity of RAM modules, chip stacking comes in handy. These stacked RAM chips are using two RAM wafers or layers that stacked on top of each other thus allows manufacturing of large DRAM modules using cheaper low density wafers. As a result, stacked chip modules are more powerful than the normal ones.

There are several types of DRAM such as:

a) Fast Page Mode (FPM)
b) Extended Data Out DRAM (EDO DRAM)
c) Burst Extended Data Out DRAM (BEDO DRAM)
d) Synchronous DRAM (SDRAM)
e) Double Data Rate Synchronous DRAM (DDR SDRAM)
f) Double Data Rate 2 Synchronous DRAM (DDR2 SDRAM)
g) Double Data Rate 3 Synchronous DRAM (DDR3 SDRAM)
h) Rambus DRAM (RDRAM)
i) Video RAM (VRAM)
j) Windows RAM (WRAM)
k) Synchronous Graphics RAM (SGRAM)

DRAM is normally used in the game gadget such as playstation, personal computers and workstation because it is cheap.

a. Fast Page Mode (FPM)

FPM was introduced in 1987. It allows faster access to data that

located within the same row. With FPM, the memory controller knows ahead of time to look in the pages of addressed memory after the CPU's write or read requests. Therefore, it reduces the waiting period for the memory controller to take instructions from the CPU and read from or write to memory. It is normally used in 486-computer system.

b. Extended Data Out DRAM (EDO DRAM)

Introduced in 1995, with an improvement in performance of 10% to 15%. This is because it requires only one CPU wait state. EDO DRAM is used in early Pentium computer.

c. Burst Extended Data Out DRAM (BEDO DRAM)

This is an upgraded model of EDO. BEDO DRAM shows an increase of 13% in performance due to it zero wait state.

d. Synchronous DRAM (SDRAM)

SDRAM is faster and more expensive than the other DRAM with speeds of 66MHz, 100MHz, 133MHz, 200MHz and 266MHz. It was introduced in 1996 and marked the first memory chip to used MHz instead of nanosecond. It does not require refreshing. SDRAM retains memory and synchronizes itself with the timing of the CPU. It involves burst mode functions and interleaving process. Interleaving process is a process whereby the CPU alternates between two or more memory banks. Each time the CPU addresses a memory bank, the memory bank need about one clock cycle. Therefore, the CPU can address the second memory bank while the first one is resetting thus saving the processing time.

SDRAM is commonly found in Pentium or Celeron system. There are 4 versions of SDRAM:

i) Double Data Rate DRAM (DDR RAM)

DDR RAM was introduced in 2000. It offers greater bandwidth by transferring data on both rising and falling edges of the clock signal.

It doubles the transfer rate without increasing the frequency of the front side bus. It prefetch buffer is 2 bits. It also operates at a lower voltage of 2.5 V compared to 3.3 V for SDRAM thus reducing the power usage. Several of DDR DRAM chips allow the use of advanced error correction features such as Chipkill, memory scrubbing and Intel SDDC.

There is another version of DDR DRAM namely Mobile DDR SDRAM (MDDR). It is used in portable devices such as digital audio player, handphone, etc. It operates at lower power usage of 1.8 V.

ii) Double Data Rate 2 DRAM (DDR2 DRAM)

This is an upgraded version of DDR DRAM. It effective clock speeds higher than DDR RAM. It was formally introduced in 2004 as a module with the lower latencies. It prefetch buffer is 4 bits. The model comes with the clock rate of 400MHz and above.

iii) Double Data Rate 3 DRAM (DDR3 DRAM)

The prototype was announced in 2005 and expected to be in the market middle of this year. The successor of DDR2 DRAM is expected to reduce the power consumption by 40% indirectly prolong the battery life. It operates at 1.5 V and will be using dual-gate transistors in order to reduce the current leakage. It prefetch buffer width is 8 bits doubling the previous version. It could transfer data at the effective clock rate of 400Mhz to 800MHz and has higher bandwidth of 1600MHz.

iv) Rambus DRAM (RDRAM)

RDRAM was introduced in 1999 by Rambus Inc. It was introduced to support PC-800 that operated at 400MHz and a maximum bandwidth of 6400MB/s. RDRAM can achieve such speed by synchronizing directly with the memory bus instead of the motherboard bus.

However, it modules came out in varieties and it also shows significant increased latency, heat output and costly. These are the reasons why manufacturers in the industry have neglect RDRAM for many years. RDRAM is being used in Intel's Pentium 4 system

many years. RDRAM is being used in Intel's Pentium 4 system.

v) Video RAM (VRAM)

VRAM is specifically designed as a video memory. It acts as a buffer between the CPU and the monitor of a computer. With it two separate access paths or dual ports, both devices are able to access VRAM at the same time. VRAM also results in better resolution and color scale. VRAM does not need to be refreshed as frequent as DRAM.

vi) Windows RAM (WRAM)

WRAM is similar to VRAM in the sense that it takes advantage of using the dual ports of VRAM to spare more rooms for memory address storage thus resulting in better color depth and video resolution. It is also much faster than VRAM.

vii) Synchronous Graphics RAM (SGRAM)

SGRAM uses it own program instructions, called blocked write and masked write commands to provide better throughput for graphic-extensive applications. It is synchronized with the CPU clock speed and is able to support up to 100 MHz.

viii) Graphics Double Data Rate 3 DRAM (GDDR3)

ATI Technologies as a graphic-card memory introduced GDDR3. GDDR3 has reduced it power and heat dispersal requirement to boost the speed of its memory modules and simplified cooling system. It also uses internal terminators to handle any graphic demands. It can transfer 4 bits of data per pin in 2 clock cycles therefore improving the bandwidth. GDDR3 was used in Radeon x800 cards, Sony Playstation 3 and Microsoft Xbox as a video memory.

ix) Graphic Double Data Rate 4 DRAM (GDDR4)

This is the successor of GDDR3 and was introduced in 2005 with more new features such as data bus inversion and multi-preamble to

more new features such as data bus inversion and multi-preamble to reduce any delay in data transmission. It prefetch buffer was increase to 8 bits. The maximum memory banks are also increased to 8. It is operated at 1.5 V. It is intended to run at a speed of 1.4 GHz.

GDDR4 2.0 GHz is made available in the market, with the clock rates of 650 MHz core. While running at 2.4 Gbits/s, it has reduced the power consumption by another 45% compared to its predecessor.

Currently, GDDR4 is used in both Nvidia and AMD graphic card.

x) Graphics Double Data Rate 5 DRAM (GDDR5)

This graphic-card memory is currently under designing phase. It will open up a new way of using DRAM and at the same time to maintain a very good backwards compatibility.

2. EMBEDDED DRAM (eDRAM)

Embedded DRAM (eDRAM) is a capacitor-based DRAM. It differs from DRAM because eDRAM is integrated on the same die or in the same package as the main ASIC or processor. It also allows much wider busses and higher operation speeds.

EDRAM can be easily found in many game consoles such as Sony Playstation, Nintendo Wii, etc. However due to it architecture where dies have to be packaged in one chip, it caused eDRAM more expensive.

3. STATIC RANDOM ACCESS MEMORY (SRAM)

SRAM can hold its data as long as the power remains on without the needs to be frequently refreshed. In term of its architecture, the symmetric structure of SRAM allows for differential signaling which enable detection of small voltages.

Although it is faster and easier to control, and also less power consumption than DRAM, it is more expensive. It complex internal

consumption than DRAM, it is more expensive. It complex internal structure makes SRAM less dense than DRAM. As a result, SRAM is not suitable for a high-capacity and low-cost application such as main memory in personal computer.

It is used for general purpose with asynchronous and synchronous interface. It can also be used as a primary cache in a powerful processor such as x86 model, microcontroller, etc.

SRAM is also used in appliances, toys, digital cameras, routers, workstation and many others. It has eased the interfacing because there is no refresh cycle plus the address and data buses can be accessed directly rather than multiplexed. It also requires only 3 controls, which are chip enable, write enable and output enable.

There are 3 types of SRAM:

1) by transistor type:

a) Bipolar function transistor is very fast but it consumes more power.

b) MOSFET consumes less power and is used in CMOS.

2) by function - asynchronous and synchronous interface.

3) by feature:

a) Zero bus turnaround where the turnaround between write and read is 0.

b) Synchronous-burst where SRAM speed up the write operation to SRAM.

4. 1T-SRAM

Introduced by Monolithic System Technology Inc. in early 1990s. This is an embedded-DRAM on a conventional digital-logic ASIC process. It combines the high-speed of SRAM with high bit-density and lower consumption of embedded DRAM. 1T-SRAM can be found

and lower consumption of embedded DRAM. 1T-SRAM can be found on foundry process such as NEC, UMC, etc.

1T-SRAM is an alternative to eDRAM. Although it delivers almost the same bit/area density, 1T-SRAM is certainly faster than eDRAM.

5. ZERO CAPACITOR RAM (ZRAM)

Developed by Innovative Silicon Inc., ZRAM single transistor performance is similar to the standard six-transistor SRAM cell used in cache memory thus offers higher density. It is also denser than the conventional one-transistor one capacitor DRAM used in computer's main memory.

It cell size is also small which make ZRAM faster than SRAM and DRAM.

6. Twin Transistor RAM (TTRAM)

TTRAM is similar to one-capacitor DRAM concept but it eliminates the capacitor by relying on the floating body effect inherent in silicon on insulator (SOI) manufacturing process. The effect caused capacitance to build up between the transistors and the underlying substrate. A transistor created using the SOI process is smaller than a capacitor, higher density than DRAM and cheap.

7. FERROELECTRIC RAM (FeRAM)

This is a non-volatile memory. Non-volatile memory means that the memory is able to retain the data stored even if power off. For many years, read only memory (ROM) has been in the list of the non-volatile memory. However, since the computer technology is progressing, RAM is also evolving into its new dimension. Though Flash RAM is dominating the current market nowadays, FeRAM definitely has few advantages over it. FeRAM is using a ferroelectric layer in order to achieve non-volatility. It consumes lower power usage, faster write speed and maximum number of write-erase cycles.

cycles.

8. MAGNETORESISTIVE RAM (MRAM)

The first MRAM chip was formally introduced in 2003. Since then, much effort has been put to develop MRAM. MRAM is based on a magnetic effect where it reads the memory using magneto-restrictive effect that allows it to read with much lower power and non-destructively. MRAM differs from the other normal RAM where its data is not stored as an electric charge or current flows but by magnetic storage elements. It small size indicates that more cells can be packed onto one single chip therefore MRAM is less expensive.

MRAM also requires no refresh at any time. It has eliminates the difference of power consumption between write and read process thus expected to reduce by 99% of DRAM power usage.

In term of speed, it is similar to SRAM but much faster than Flash memory while suffers no degradation over time compared to Flash memory itself.

MRAM is proposed to be used in notebooks, handphones, digital cameras, personal computer, aerospace and military systems and many others.

9. PHASE-CHANGE MEMORY RAM (PRAM)

PRAM is using the same manufacturing technology of **Chalcogenide RAM** (CRAM). CRAM was first discovered in 1960 based on the material used namely chalcogenide glass. Chalcogenide glass contains an alloys of germanium, antimony and tellurium, of which upon application of heat at certain level will switched between two states, crystalline and amorphous. The switching process between the two states is very fast which caused changes to the electrical resistance.

PRAM offers much higher performance in applications where fast writing is utmost important. it is thousand of times faster than the conventional hard drives. PRAM can be constructed using diodes

instead of transistors which will further reducing the cost of making PRAM since diode is smaller and cheaper than a transistor.

PRAM may be used in aerospace and military industries due to its excellent radiation tolerance and latch up immunity.

10. Semiconductor-Oxide-Nitride-Oxide-Semiconductor (SONOS)

SONOS is very similar to Flash but is much easier to produce. It can be built at a smaller scale than Flash with lower size of the insulator layer. The voltage required for write process is much lower between 5 V to 8 V compared to Flash, which is 9 V to 20 V.

However SONOS is still under ongoing research by several manufacturers, to be used for tasks related to military and space systems.

11. Resistive RAM (RRAM)

Developed by Sharp, it is said to be 100 times faster than the current Flash memory.

12. Nano-RAM (NRAM)

Developed based on Nantero Technology, it is built by depositing masses of nanotubes on a pre-fabricated chip containing rows of bar-shaped electrodes with the slightly taller insulating layers between them.
NRAM has a density similar to DRAM with smaller size of terminals and electrodes. As a result, it is less expensive. It does not require power to refresh it and the memory remains still even if the power is off. It also consume less power to run and therefore much faster than DRAM. The read and write process consume low energy compared to Flash thus prolonging the battery life.

NRAM is said to be soon replacing Flash, DRAM and SRAM.

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Initially, main memory systems were built from the vacuum tubes and its core used wires threaded through small ferrite electromagnetic ball. As this memory evolved through time, another type of volatile memory called RAM was produced with integrated circuits. Later on, non-volatile RAM has been developed where it can preserve data while power is off. This technology is based on magnetic tunnel effect and carbon nanotubes.

Based on their features, each of the above RAM is useful to certain types of computer systems. It performance is measured based on its density, packaging, capability and speed.
From DRAM to NRAM, each of them has its own advantages and disadvantages. The comparisons with the other systems have been laid down in this report as a guidance to determine the types of RAM that suitable with a particular class of computer system. Some of it is still under ongoing researches and designing phases.

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